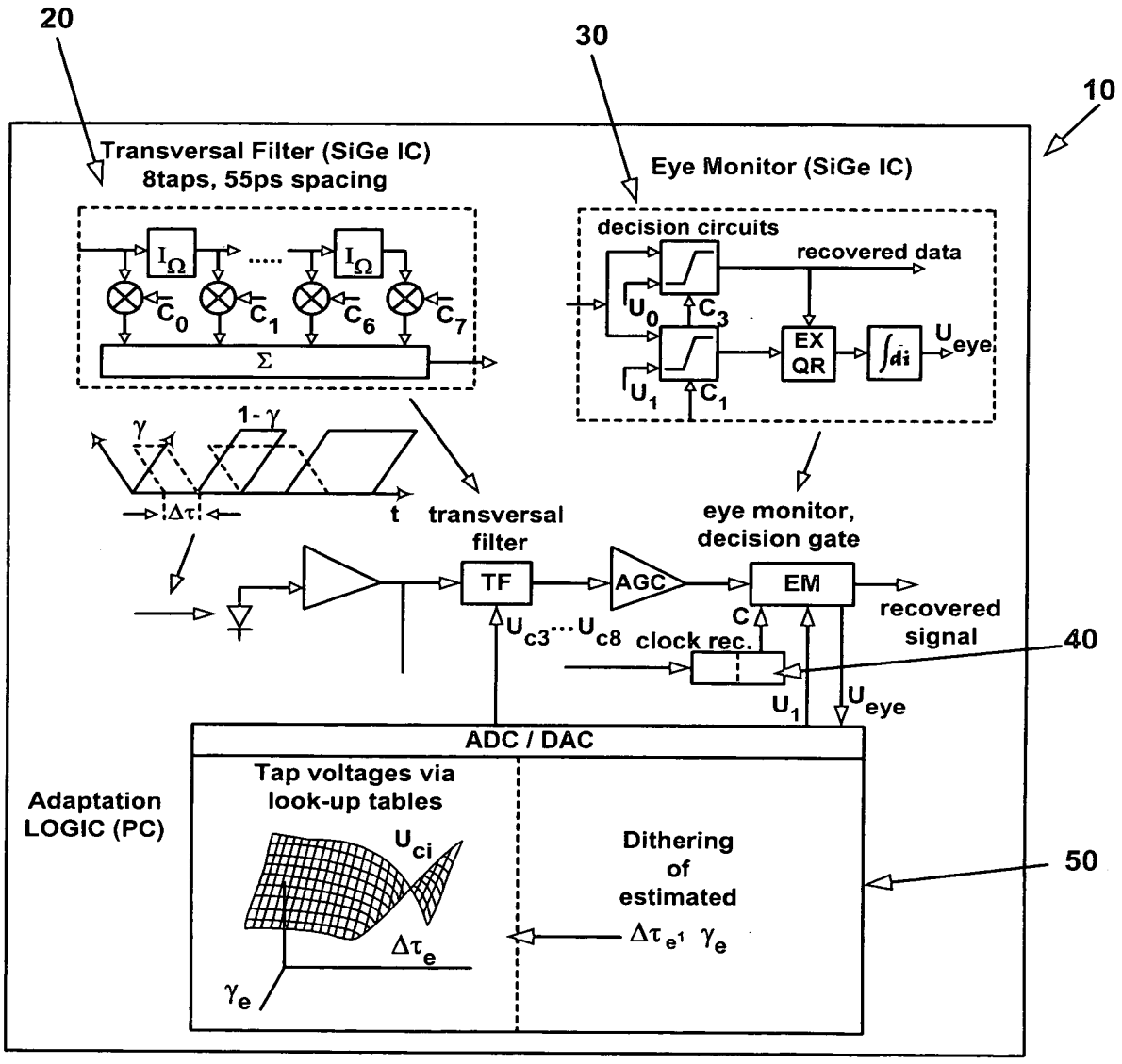

FIG. 1 (Prior Art)

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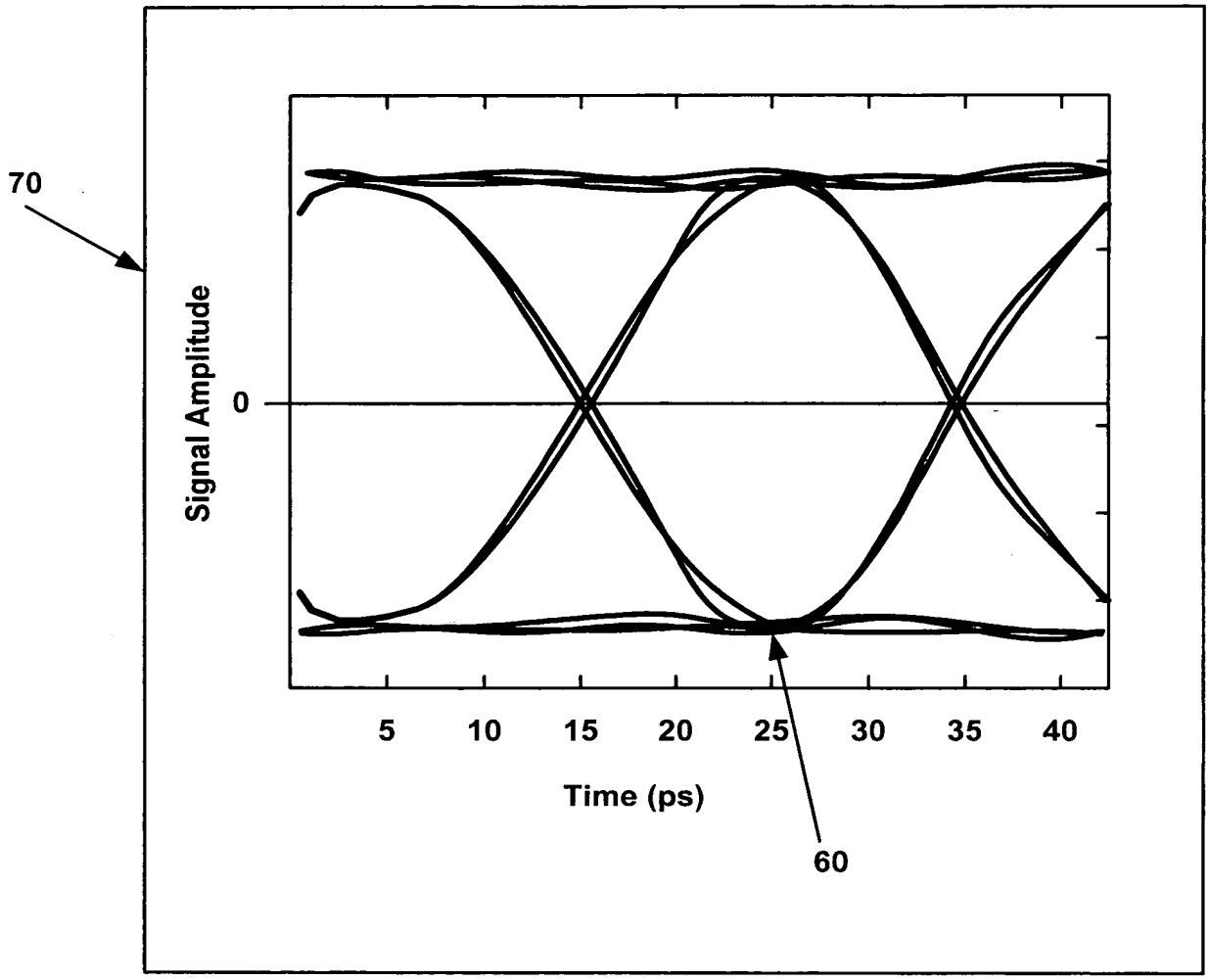

FIG. 2A (Prior Art)

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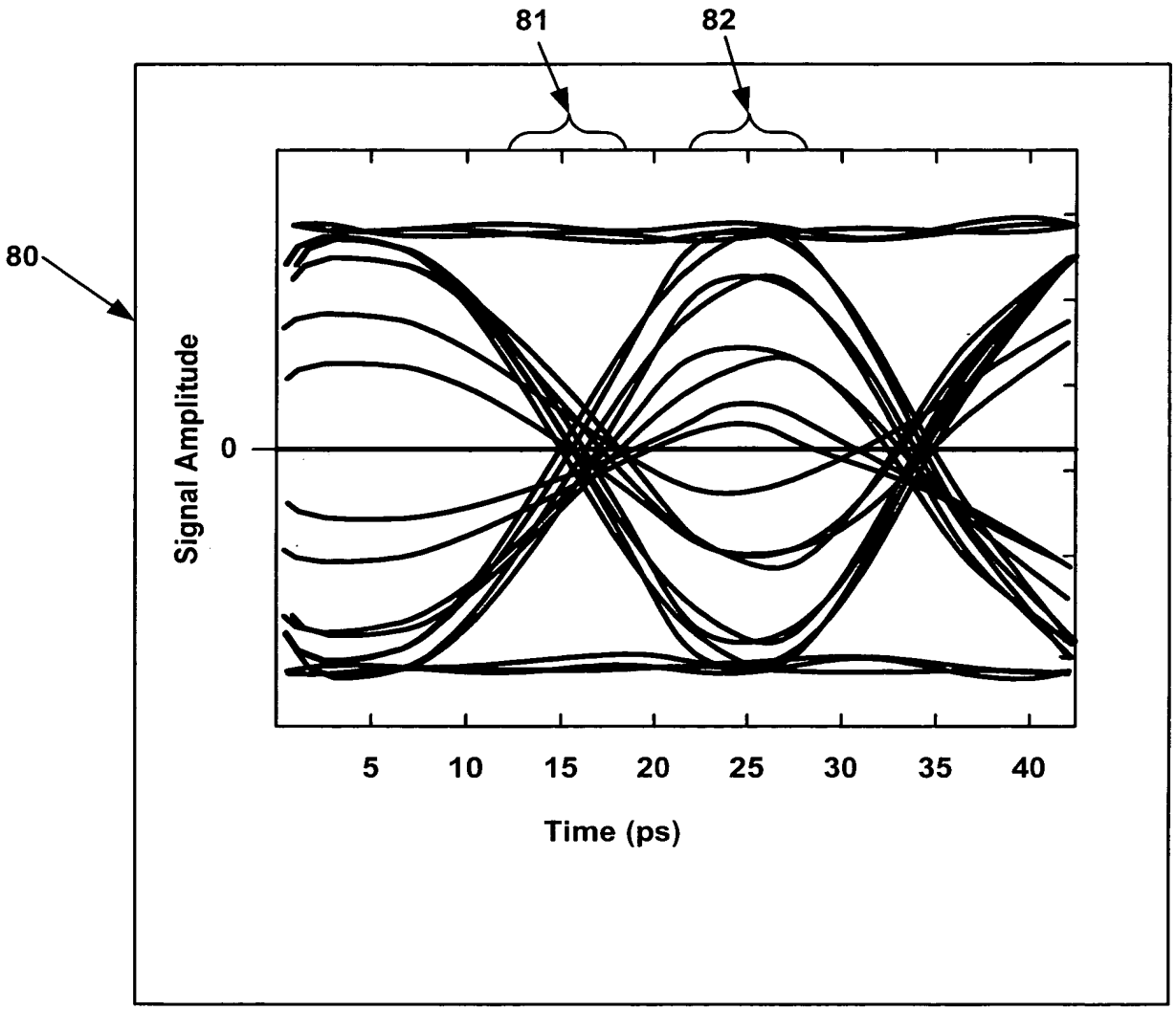

FIG. 2B (Prior Art)

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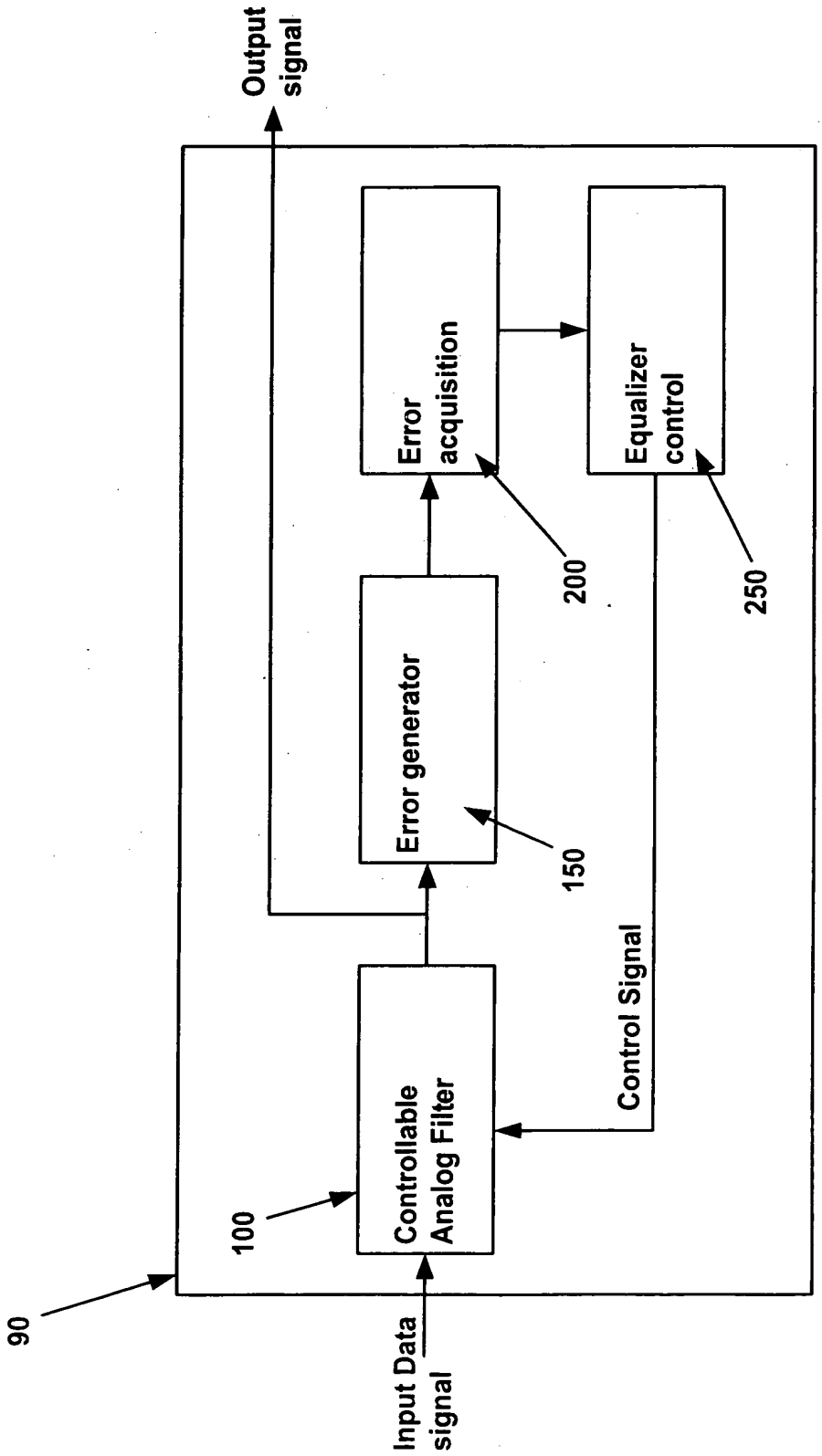
Output signal
Error acquisition
Equalizer control
200
250
Error generator
150
Control Signal
Controllable Analog Filter
100
90
Input Data signal

FIG. 3

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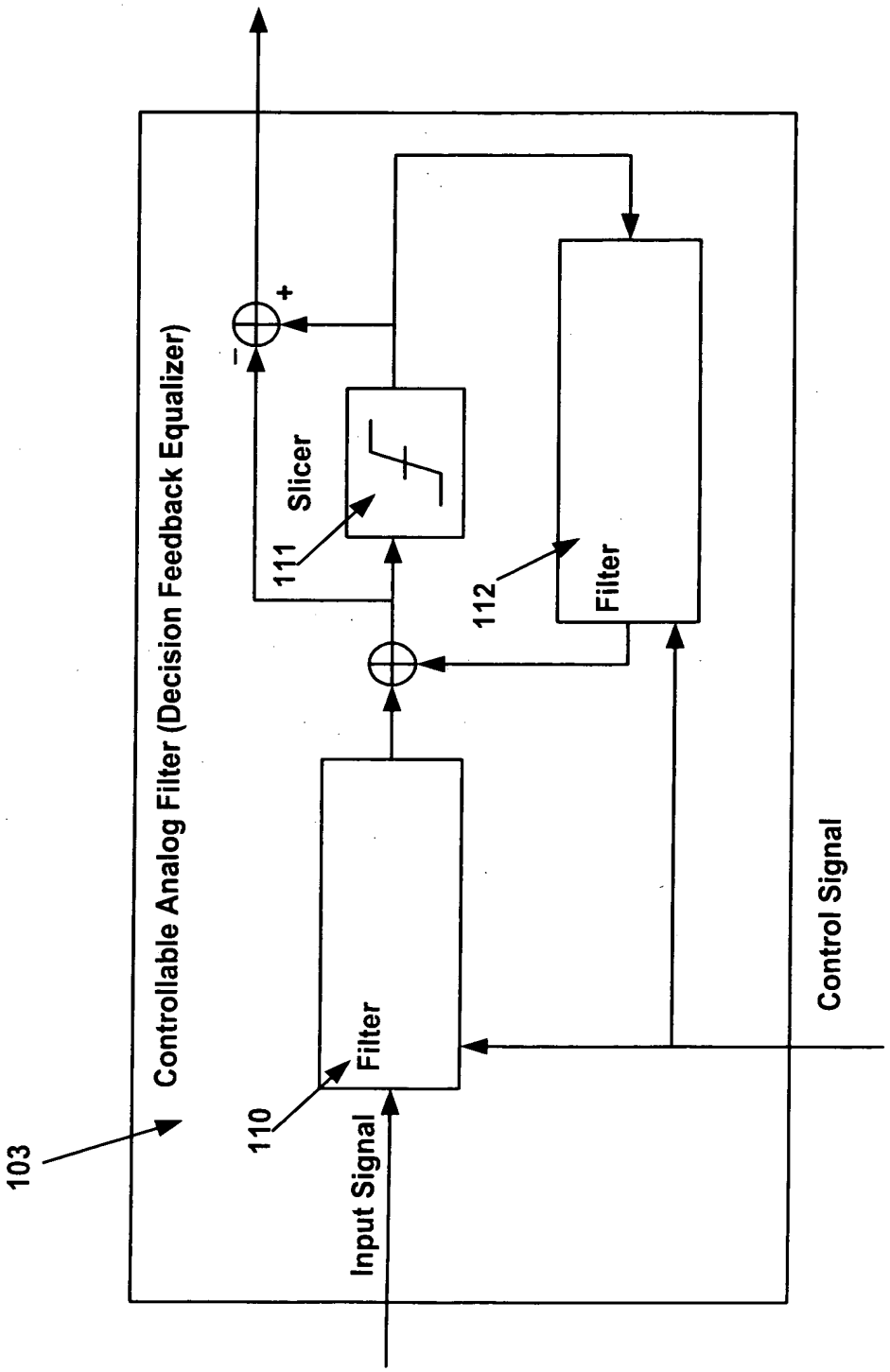
Controllable Analog Filter (Decision Feedback Equalizer)
103
110
Filter
Input Signal
111
Slicer
112
Filter
+
-
Control Signal

FIG. 4

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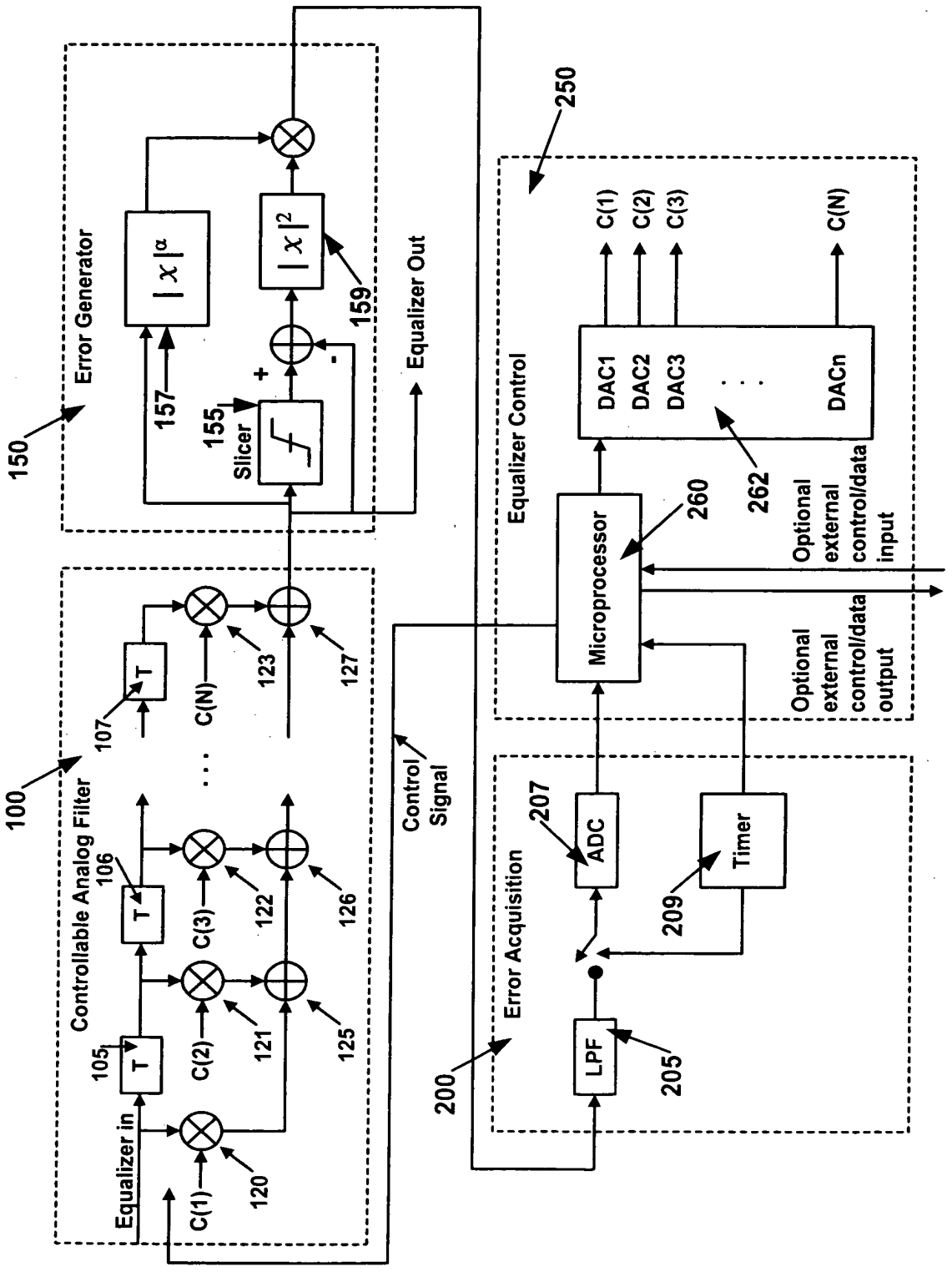
Error Generator
150
157
155
Slicer
159
Equalizer Out
250
Equalizer Control
C(1)
C(2)
C(3)
C(N)
DAC1
DAC2
DAC3
DACn
262
260
Microprocessor
Optional external control/data input
Optional external control/data output
Control Signal
100
Controllable Analog Filter
107
106
105
123
122
121
127
126
125
120
Equalizer in
C(1)
C(2)
C(3)
C(N)
T
200
Error Acquisition
207
ADC
209
Timer
LPF
205

FIG. 5

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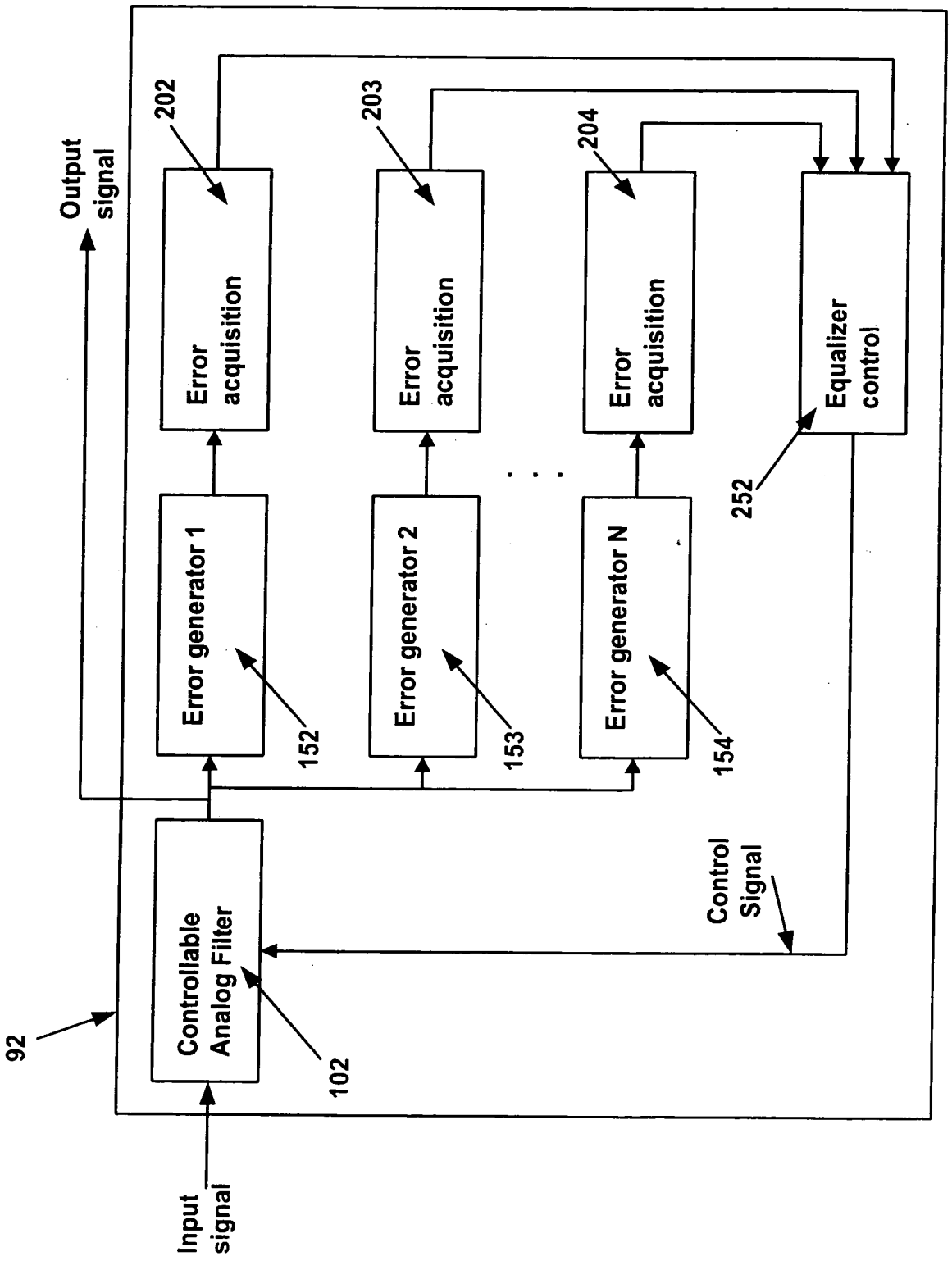
Output signal
202
203
204
Error acquisition
Error acquisition
Error acquisition
Equalizer control
252
Error generator 1
Error generator 2
Error generator N
152
153
154
Control Signal
Controllable Analog Filter
102
92
Input signal

FIG. 6

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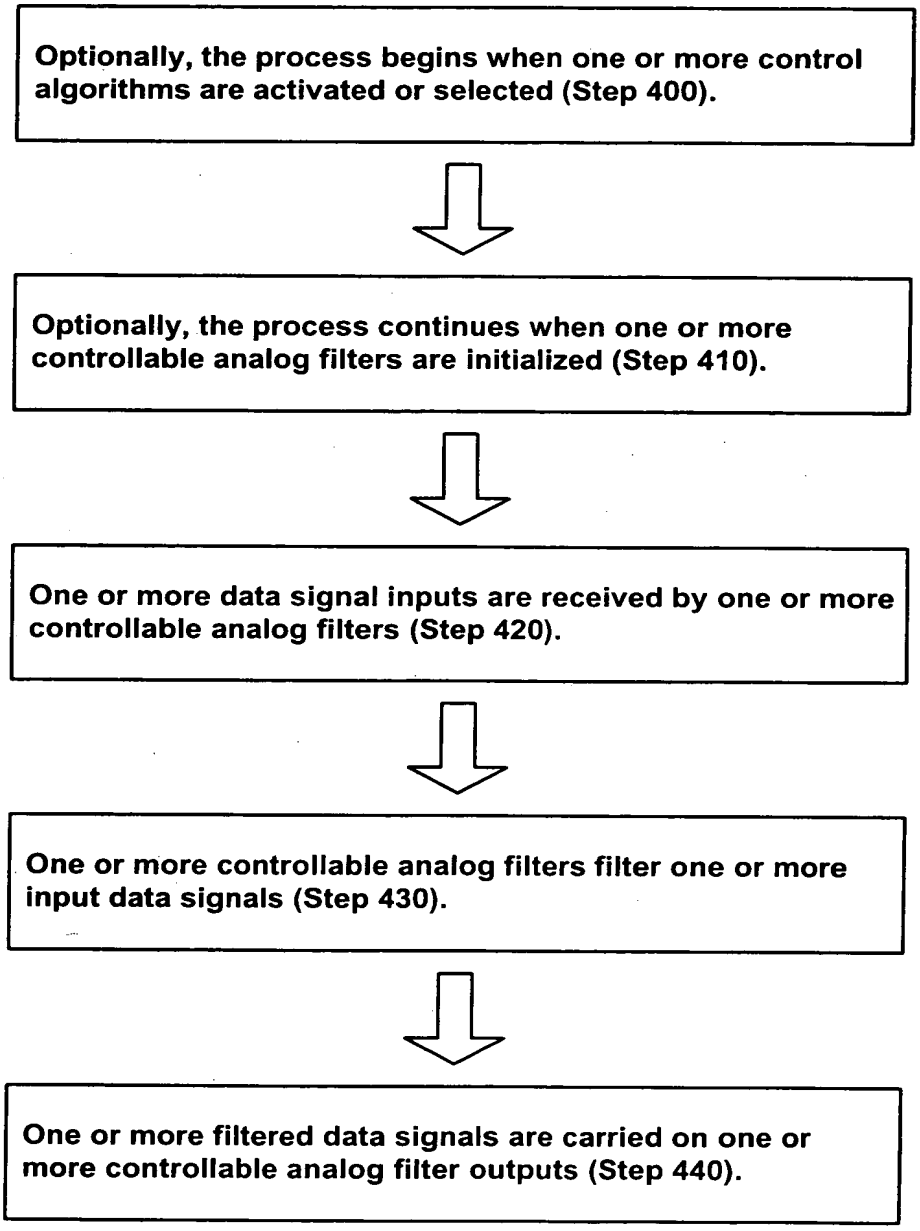
Optionally, the process begins when one or more control algorithms are activated or selected (Step 400).
Optionally, the process continues when one or more controllable analog filters are initialized (Step 410).
One or more data signal inputs are received by one or more controllable analog filters (Step 420).
One or more controllable analog filters filter one or more input data signals (Step 430).
One or more filtered data signals are carried on one or more controllable analog filter outputs (Step 440).

FIG. 7A

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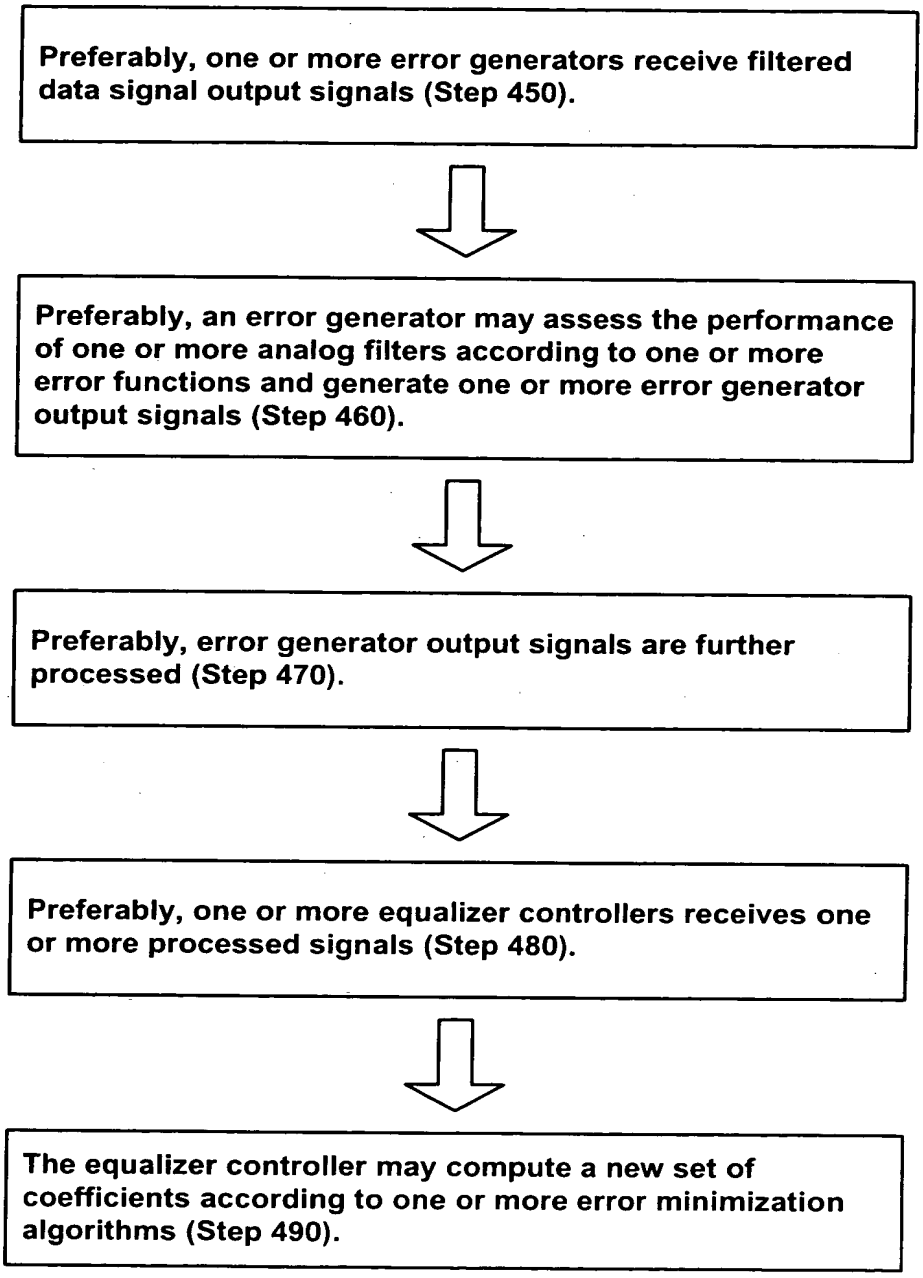
Preferably, one or more error generators receive filtered data signal output signals (Step 450).
Preferably, an error generator may assess the performance of one or more analog filters according to one or more error functions and generate one or more error generator output signals (Step 460).
Preferably, error generator output signals are further processed (Step 470).
Preferably, one or more equalizer controllers receives one or more processed signals (Step 480).
The equalizer controller may compute a new set of coefficients according to one or more error minimization algorithms (Step 490).

FIG. 7B

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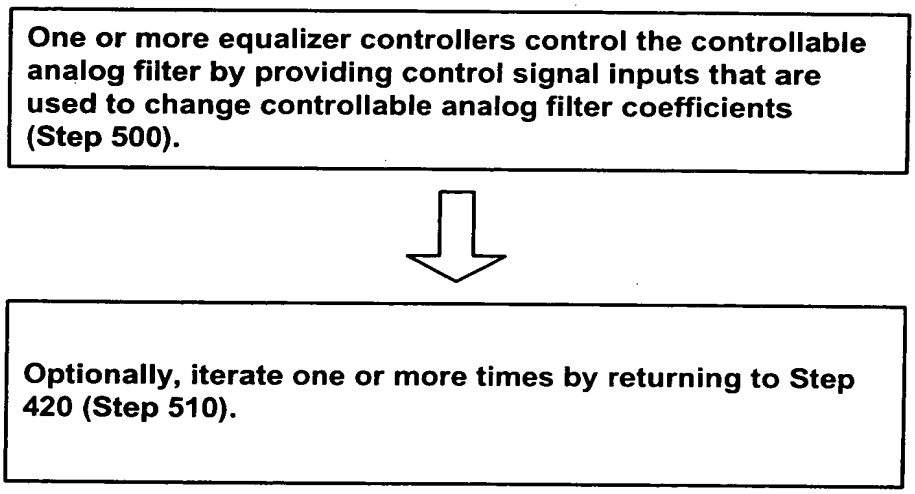
One or more equalizer controllers control the controllable analog filter by providing control signal inputs that are used to change controllable analog filter coefficients (Step 500).
Optionally, iterate one or more times by returning to Step 420 (Step 510).

FIG. 7C

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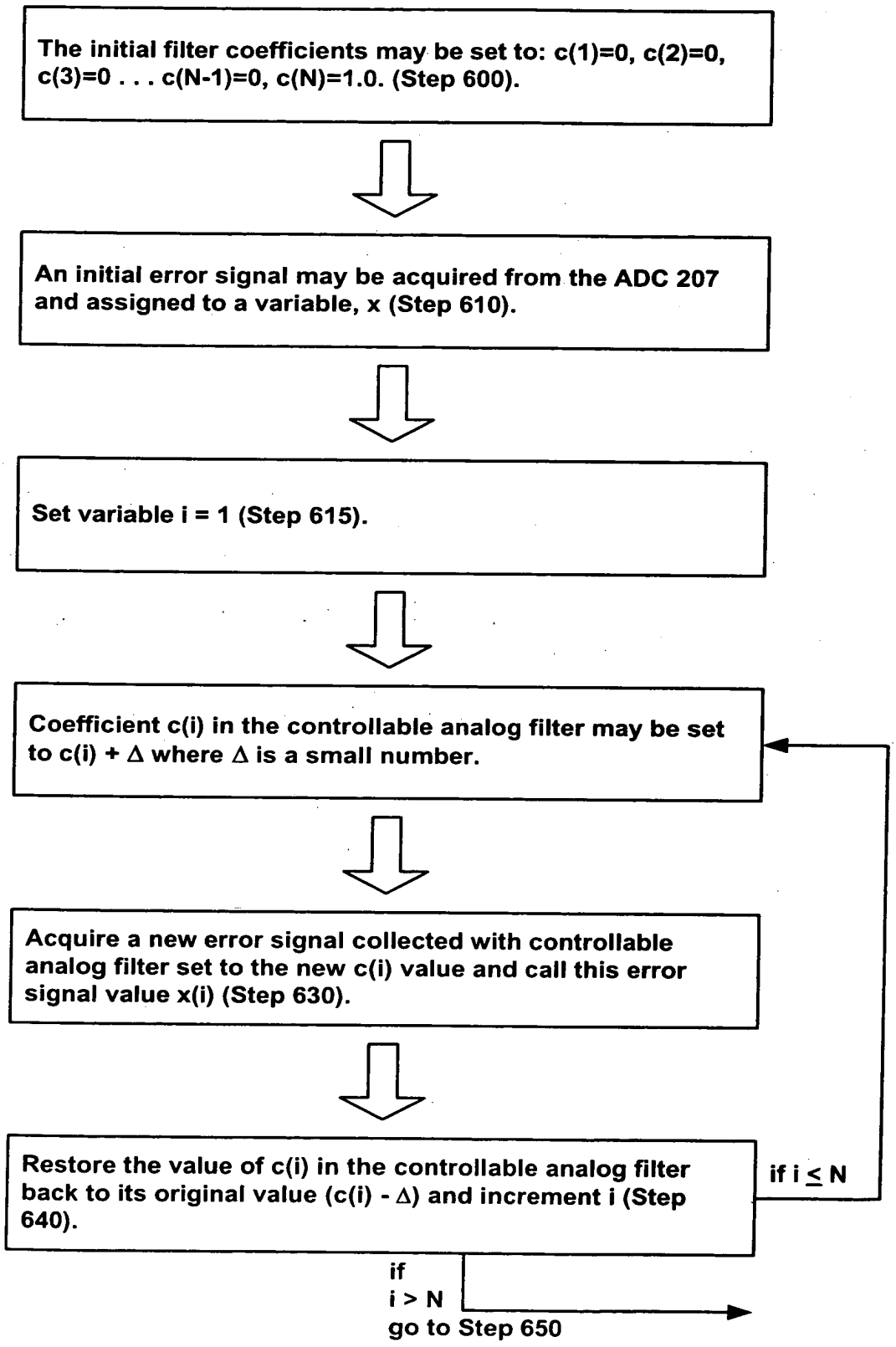
The initial filter coefficients may be set to: c(1)=0, c(2)=0, c(3)=0 . . . c(N-1)=0, c(N)=1.0. (Step 600).
An initial error signal may be acquired from the ADC 207 and assigned to a variable, x (Step 610).
Set variable i = 1 (Step 615).
Coefficient c(i) in the controllable analog filter may be set to c(i) + Δ where Δ is a small number.
Acquire a new error signal collected with controllable analog filter set to the new c(i) value and call this error signal value x(i) (Step 630).
Restore the value of c(i) in the controllable analog filter back to its original value (c(i) - Δ) and increment i (Step 640).
if i ≤ N
if i > N
go to Step 650

FIG. 8A

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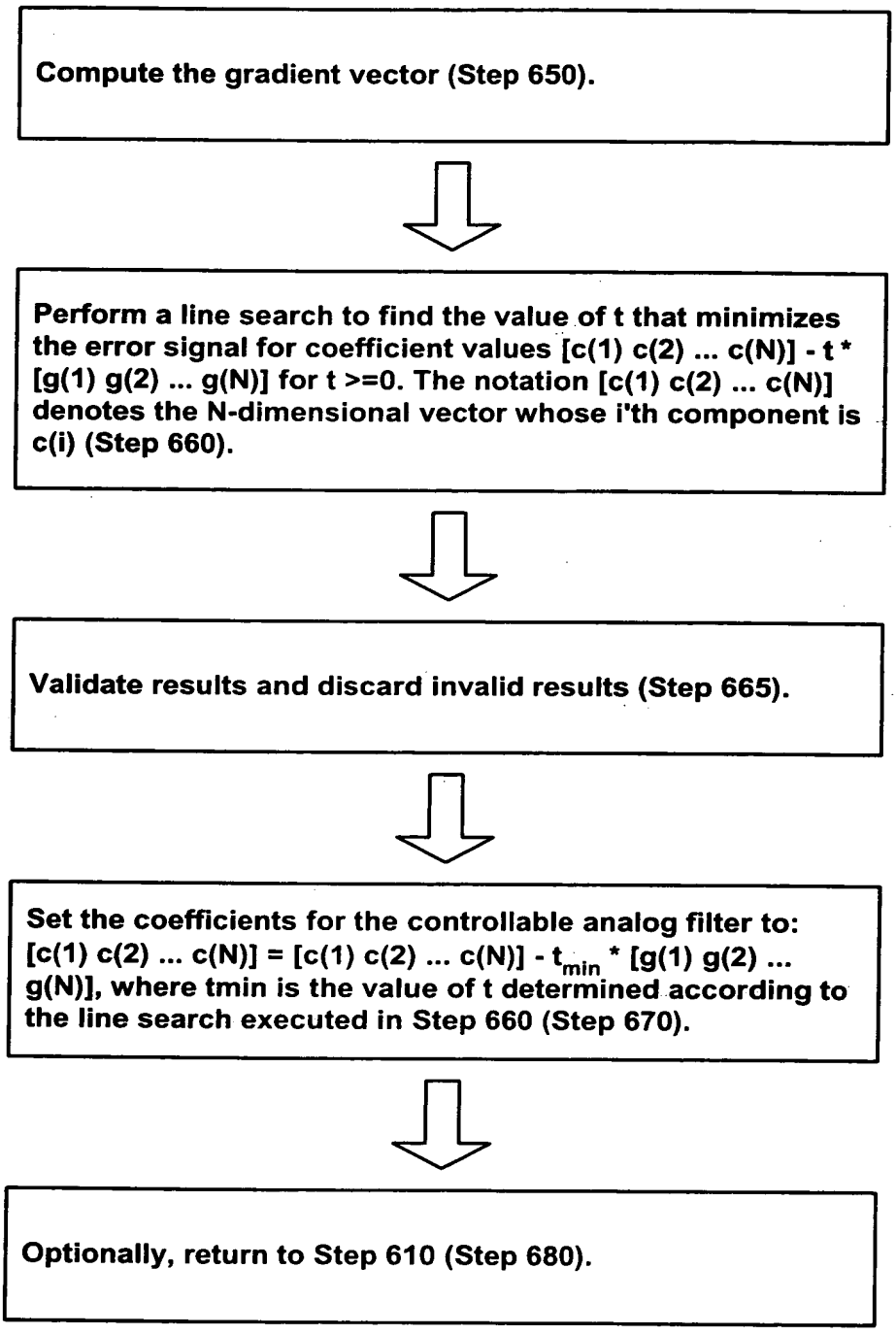
Compute the gradient vector (Step 650).
Perform a line search to find the value of t that minimizes the error signal for coefficient values [c(1) c(2) ... c(N)] - t * [g(1) g(2) ... g(N)] for t >=0. The notation [c(1) c(2) ... c(N)] denotes the N-dimensional vector whose i'th component is c(i) (Step 660).
Validate results and discard invalid results (Step 665).
Set the coefficients for the controllable analog filter to: [c(1) c(2) ... c(N)] = [c(1) c(2) ... c(N)] - t_{min} * [g(1) g(2) ... g(N)], where tmin is the value of t determined according to the line search executed in Step 660 (Step 670).
Optionally, return to Step 610 (Step 680).

FIG. 8B